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10/501384

Express Mail No. EV310 858 065US

Docket No. 035967-006

DT15 Rec'd PCT/PTO 13 JUL 2004

APPARATUS FOR CONTINUOUS PHASE QUADRATURE AMPLITUDE MODULATION AND DEMODULATION

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates to an apparatus for continuous phase quadrature amplitude modulation and demodulation, and more particularly, to an apparatus for continuous phase quadrature amplitude modulation and demodulation to continuously process phases and amplitudes at symbol change points in an M-ary quadrature amplitude modulation method.

Description of the Related Art

[0002] In general, phases are discontinuous at symbol change points in a quadature amplitude modulation method and a quadrature amplitude demodulation method. Accordingly, since a side-lobe does not drop rapidly, an adjacent channel interference occurs. In addition, since the amplitudes are discontinuous at symbol change points, a power amplifier has to quickly follow the amplitude.

SUMMARY OF THE INVENTION

[0003] To solve the above-described problems, it is an objective of the present invention to provide an apparatus for continuous phase quadrature amplitude modulation and demodulation to improve a spectrum efficiency by making the phases continuous at symbol change points of a quadrature amplitude modulation signal.

[0004] To solve the above-described problems, it is another objective of the present invention to provide an apparatus for continuous phase quadrature amplitude modulation and demodulation to reduce an adjacent channel interference by improving the roll-off speed of a side-lobe.

[0005] To solve the above-described problems, it is still another objective of the present invention to provide an apparatus for continuous phase quadrature amplitude modulation and demodulation to reduce loads of a power amplifier by making the changes continuous in amplitude at symbol change points.

[0006] To meet the above objective, according to one aspect of the present invention, there is provided an apparatus for continuous phase quadrature amplitude modulation and demodulation comprising a continuous phase quadrature modulator having a first multiplier multiplying an I-channel by a cosine wave weighted function, a second multiplier multiplying an output signal of the first multiplier by a cosine wave of a carrier frequency, a delay delaying a Q-channel by a predetermined time, a third multiplier multiplying the Q-channel by a sine wave weighted function, a fourth multiplier multiplying an output signal of the third multiplier by the sine wave of the carrier frequency, and an adder adding an output signal of the second multiplier and an output signal of the fourth multiplier; and a continuous phase quadrature demodulator having a fifth multiplier multiplying the I-channel by the cosine wave of the carrier frequency, a sixth multiplier multiplying a signal from the fifth multiplier by the cosine wave weighted function, a first integrator and sampler integrating a signal from the sixth multiplier for the symbol duration time, a seventh multiplier multiplying the Q-channel by the sine wave of the carrier frequency, an eighth

multiplier multiplying a signal from the seventh multiplier by the sine wave weighted function, and a second integrator and sampler integrating a signal from the eighth multiplier by the symbol duration time.

[0007] It is preferable that the apparatus further comprises a signal mapper that separates a received binary data to the I-channel and the Q-channel and outputs the I-channel and the Q-channel to the first multiplier and the delay, respectively.

[0008] It is preferable that the apparatus further comprises a first oscillator that outputs the cosine wave weighted function.

[0009] It is preferable that the apparatus further comprises a first phase shifter that phase-shifts the cosine wave weighted function output from the first oscillator by 90 degrees and outputs the sine wave weighted function.

It is preferable that the cosine wave weighted function is $\cos w_i t$.

It is preferable that the cosine wave of the carrier frequency is $\cos w_c t$.

[0010] It is preferable that the predetermined time is the half of a symbol duration time.

[0011] It is preferable that the apparatus further comprises a second oscillator that outputs the cosine wave of the carrier frequency.

[0012] It is preferable that the apparatus further comprises a second phase shifter that phase-shifts the cosine wave of the carrier frequency output from the second oscillator by 90 degrees and outputs the sine wave of the carrier frequency.

It is preferable that the sine wave weighted function is $\sin w_i t$.

It is preferable that the sine wave of the carrier frequency is $\sin w_c t$.

[0013] It is preferable that the apparatus further comprises a phase locked loop (PLL) that controls the phase of a received signal.

[0014] It is preferable that the apparatus further comprises a clock generator that receives a signal from the PLL and generates a clock cycle having a predetermined amount of time.

[0015] It is preferable that the apparatus further comprises a third phase shifter that phase-shifts the cosine wave of the carrier frequency transferred from the PLL by 90 degrees and generates the sine wave of the carrier frequency.

[0016] It is preferable that the apparatus further comprises a second oscillator that receives the clock cycle from the clock generator and outputs the cosine wave weighted function.

[0017] It is preferable that the apparatus further comprises a fourth phase shifter that phase-shifts the cosine wave weighted function from the second oscillator by 90 degrees and outputs the sine wave weighted function.

[0018] It is preferable that the apparatus further comprises a first determiner that determines an integral signal from the first integrator and sampler.

[0019] It is preferable that the apparatus further comprises a second determiner that determines an integral signal from the second integrator and sampler.

[0020] It is preferable that the apparatus further comprises a signal demapper that receives signals from the first determiner and the second determiner and outputs a binary data.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram illustrating a continuous phase quadrature amplitude modulator according to the present invention;

FIG. 2 is a block diagram illustrating a continuous phase quadrature amplitude demodulator according to the present invention; and

FIG. 3 illustrates a waveform of an output signal from the continuous phase quadrature amplitude modulator of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0022] The present invention will now be described in more detail with reference to the accompanying drawing.

[0023] FIG. 1 is a block diagram illustrating a continuous phase quadrature amplitude modulator according to the present invention, and FIG. 2 is a block diagram illustrating a continuous phase quadrature amplitude demodulator according to the present invention.

[0024] Referring to FIGS. 1 and 2, a continuous phase quadrature amplitude modulator according to the present invention includes a signal mapper 100, a first multiplier 110, a second multiplier 120, a delay 130, a third multiplier 140, a fourth multiplier 150, a first oscillator 160, a first phase shifter 170, a second oscillator 180, a second phase shifter 190, and an adder 200. A continuous phase quadrature amplitude demodulator includes a fifth

multiplier 210, a sixth multiplier 220, a first integrator and sampler 230, a first determiner 240, a seventh multiplier 250, an eighth multiplier 260, a second integrator and sampler 270, a second determiner 280, a phase locked loop (PLL) 290, a third phase shifter 300, a clock generator 310, a fourth phase shifter 320, a second oscillator 330, and a signal demapper 340.

[0025] The first multiplier 110 multiplies an I-channel by a cosine wave weighted function, and the second multiplier 120 multiplies an output signal of the first multiplier 110 by a cosine wave of a carrier frequency. The delay 130 delays a Q-channel by half of the duration of a symbol duration time, and the third multiplier 140 multiplies the Q-channel by a sine wave weighted function. The fourth multiplier 150 multiplies an output signal of the third multiplier 140 by the sine wave of the carrier frequency, and the adder 200 adds an output signal of the second multiplier 120 and an output signal of the fourth multiplier 150. Here, the signal mapper 100 separates a received binary data to the I-channel and the Q-channel and outputs the I-channel and the Q-channel to the first multiplier 110 and the delay 130, respectively. The first oscillator 160 outputs the cosine wave weighted function. The first phase shifter 170 phase-shifts the cosine wave weighted function output from the first oscillator 160 by 90 degrees to output the sine wave weighted function. The second oscillator 180 outputs the cosine wave of the carrier frequency, and the second phase shifter 190 phase-shifts the cosine wave of the carrier frequency output from the second oscillator 180 by 90 degrees to output the sine wave of the carrier frequency.

The cosine wave weighted function is $\cos w_i t$, and the cosine wave of the carrier frequency is $\cos w_c t$. The sine wave weighted function is $\sin w_i t$, and the sine wave of the carrier frequency is $\sin w_c t$.

[0026] In addition, the fifth multiplier 210 multiplies the I-channel by the cosine wave of the carrier frequency, and the sixth multiplier 220 multiplies a signal from the fifth multiplier 210 by the cosine wave weighted function. The first integrator and sampler 230 integrates a signal from the sixth multiplier 220 for the symbol duration time. The seventh multiplier 250 multiples the Q-channel by the sine wave of the carrier frequency, and the eighth multiplier 260 multiplies a signal from the seventh multiplier 250 by the sine wave weighted function. The second integrator and sampler 270 integrates a signal from the eighth multiplier 260 for the symbol duration time. PLL 290 controls the phase of a received signal, and the clock generator 310 receives a signal from the PLL 290 to generate a clock cycle for a predetermined time. In addition, the third phase shifter 300 phase-shifts the cosine wave of the carrier frequency transferred from the PLL 290 by 90 degrees to generate the sine wave of the carrier frequency, and the second oscillator 330 receives the clock cycle from the clock generator 310 to output the cosine wave weighted function. The fourth phase shifter 320 phase-shifts the cosine wave weighted function from the second oscillator 330 by 90 degrees to output the sine wave weighted function. The first determiner 240 determines an integral signal from the first integrator and sampler 230, and the second determiner 280 determines an integral signal from the second integrator and sampler 270. The signal demapper 340 receives signals from the first determiner 240 and the second determiner 280 to output a binary data.

[0027] More specifically, the continuous phase quadrature amplitude modulator of FIG. 1 maps a $\log_2 M$ bit series signal, resulting from an M-ary quarature amplitude modulation, from a mapping table to corresponding quadrature amplitude modulation signal. The

$\log_2 M$ bit series signal is divided into $\log_2 \sqrt{M}$ bits and assigned to the I-channel and the Q-channel. The I-channel signal is pulse shaped into the cosine wave weighted function of $\cos(\Pi / T_s)t$ and modulated into the cosine wave $\cos w_c t$ of the carrier frequency f_c. Here, T_s is the symbol duration time.

[0028] On the other hand, the Q-channel signal has a time offset of $T_s / 2$ from the I-channel due to the delay 130 that delays a signal by the half of the symbol duration time. The delayed signal is pulse shaped into the sine wave weighted function of $\sin(\Pi / T_s)t$ and modulated into the sine wave $\sin w_c t$ of the carrier frequency f_c. The modulated I-channel signal and the modulated Q-channel signal are added in the adder 200 and transferred through a channel. As a result, an output M-CPQAM signal continues phases and amplitudes at symbol change points to improve a frequency spectrum efficiency while reducing loads of a power amplifier (not shown).

[0029] When the continuous phase quadrature amplitude demodulator of FIG. 2 is used, the cosine signal and the sine signal transferred through the channel can be restored using the I-channel and the Q-channel because the cosine signal and the sine signal are orthogonal. First, the I-channel is multiplied by the cosine wave $\cos w_c t$ of the carrier frequency in the fifth multiplier 210 and multiplied by the sine wave weighted function of $\cos(\Pi / T_s)t$ in the sixth multiplier 220. The first integrator and sampler 230 integrates the multiplied signal and samples the integral signal to restore the signal into a base band signal corresponding to the Q-channel. Thereafter, a corresponding symbol is determined using the first determiner

240. The restored I-channel and Q-channel signals are determined into original signals using the mapping table.

[0030] FIG. 3 illustrates a waveform of an output signal from the continuous phase quadrature amplitude modulator of FIG. 1. Here, the waveform of FIG. 3 is obtained by simulating a 16-quadrature amplitude modulation signal. Referring to FIG. 3, when (3,-3), (1,-1), (3,1), and (1,-1) symbols are assigned as a 16-continuous phase quadrature amplitude modulation signal, the phases and the amplitudes are continuous at the multiple times of four, which are symbol change points. In addition, the present invention is not limited to an M-ary square quadarature amplitude modulation; however, the present invention can be applied to an optional rectangular quadrature amplitude modulation. Furthermore, the present invention can be applied to a hierarchical quadrature amplitude modulation that is proposed in digital broadcasting and other systems using I-Q modulation.

[0031] While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.

[0032] As described above, an apparatus for continuous phase quadrature amplitude modulation and demodulation according to the present invention has advantages as follows.

[0033] The apparatus for continuous phase quadrature amplitude modulation and demodulation improves a spectrum efficiency by making the phases and amplitudes continuous at symbol change points of a quadrature amplitude modulation signal, reduces an

adjacent channel interference by improving the roll-off speed of a side-lobe, and reduces loads of a power amplifier.

[0034] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the spirit and scope of the present invention as defined by the following claims.